A Fully integrated D-band Direct-Conversion I/Q Transmitter and Receiver Chipset in SiGe BiCMOS Technology

Sona Carpenter, Herbert Zirath, IEEE, Fellow, Zhongxia Simon He, Mingquan Bao

Abstract: **This paper presents design and characterization of single-chip 110–170 GHz (D-band) direct conversion in-phase/quadrature-phase (I/Q) transmitter and receiver monolithic microwave integrated circuits (MMICs), realized in a 130 nm SiGe BiCMOS process with ft/fmax of 250 GHz/370 GHz. The chipset is suitable for low power wideband communication and can be used in both homodyne and heterodyne architectures. The Transmitter chip consists of a six-stage power amplifier, an I/Q modulator, and a LO multiplier chain. The LO multiplier chain consists of frequency sixtupler followed by a two-stage amplifier. It exhibits a single sideband conversion gain of 23 dB and saturated output power of 0 dBm. The 3 dB RF bandwidth is 31 GHz from 114 to 145 GHz. The receiver includes a low noise amplifier, I/Q demodulator and x6 multiplier chain at the LO port. The receiver provides a conversion gain of 27 dB and has a noise figure of 10 dB. It has 3 dB RF bandwidth of 28 GHz from 112-140 GHz. The transmitter and receiver have dc power consumption of 240 mW and 280 mW, respectively. The chip area of each transmitter and receiver circuit is 1.4 mm $\times$ 1.1 mm.**

Index Terms: **Demodulator, direct conversion, I/Q transceiver, low noise amplifier, measurement, millimeter wave integrated circuits, mixer, modulator, multiplier, MMICs, power amplifier, wireless communication.**

I. INTRODUCTION

WITH the growing demand of high data rate communication, millimeter wave and sub-millimeter-wave frequency ranges have significantly become an important research area [1], [2]. These spectrum ranges allow for the much higher fractional bandwidth and highly integrated millimeter wave and terahertz systems using either a simple modulation scheme such as ASK and OOK or a high order modulation scheme such as QPSK and QAM [3]. For instance, D-band offers opportunities for new applications in low-cost silicon technology, such as high-resolution millimeter-wave imaging [4], and high-speed point-to-point telecommunication links [5], [6], 122.5–GHz industrial–scientific–medical (ISM) band short range radar [7], [8]. Recently, the Federal Communications Commission (FCC) announced new frequency band of 141–148.5 GHz for fixed and mobile point-to-point high bandwidth wireless links [9]. In D-band, the low atmospheric attenuation (below 1 dB/km) window (120–160 GHz) is suitable for medium range backhaul gigabit communication [10] and high atmospheric attenuation points at 118 GHz (resonance of O2 molecule) and at 183 GHz (resonance of H2O molecule) can be used for secure high-speed short-range communication. Most importantly beyond 100 GHz, integration of antennas becomes possible due to the small operating wavelengths [11]–[13]. This simplifies the packaging process and enables a fully integrated low-cost transceiver solutions for dense urban small cell areas. Alternatively, gigabit-rate wired communication can be performed in D-band using dielectric waveguide as a transmission medium. From our perspective, this frequency band offers a good compromise between availability of the latest semiconductor process developments and low-cost production solutions.

One of the main challenges of D-band generic front-end design is to realize wideband RF building blocks and correspondingly monolithic integrated transmitters and receivers that cover multiple frequency bands. So far, different publications have been reported in literature based on application specific implementations [14]–[25]. However, with the relatively low cut-off frequency of the transistors in silicon process technologies, it is not easy to design an integrated transceiver beyond 100 GHz, where the operating frequency reaches to about one-third of fmax [15].

Recently several transmitter and receiver architectures have been demonstrated for operating frequencies above 100 GHz. The transmitters are typically realized based on a frequency multiplier [17], [18], [20], [25] or mixer topology [15], [19], [22]. The former utilizes a multiplier immediately before the antenna while the latter adopts a mixer followed by a power amplifier. On the other hand, in the receiver side, commonly a low noise amplifier together with a mixer is employed at the front-end [14], [15], [19], [22]. However, as the frequency goes up close to the fmax of technology, the frequency conversion is performed upfront, making a mixer-first architecture [16], [18], [21], [25]. The LO chain is also realized using either a high frequency VCO or a frequency multiplier, where multipliers are beneficial in terms of wide tuning range and relaxed phase noise performance [19]. Various kinds of mil-

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Sona Carpenter is with Sivers Semiconductors AB, Sweden (e-mail: carpentersona@gmail.com). Herbert Zirath, Zhongxia Simon He are with the Department of Microtechnology and Nanoscience, MC2, Chalmers University of Technology, 41296, Göteborg, Sweden. M. Bao is with Microwave System Radio Access Hardware, Device and EMF, Ericsson Research, Ericsson AB, Göteborg, Sweden.

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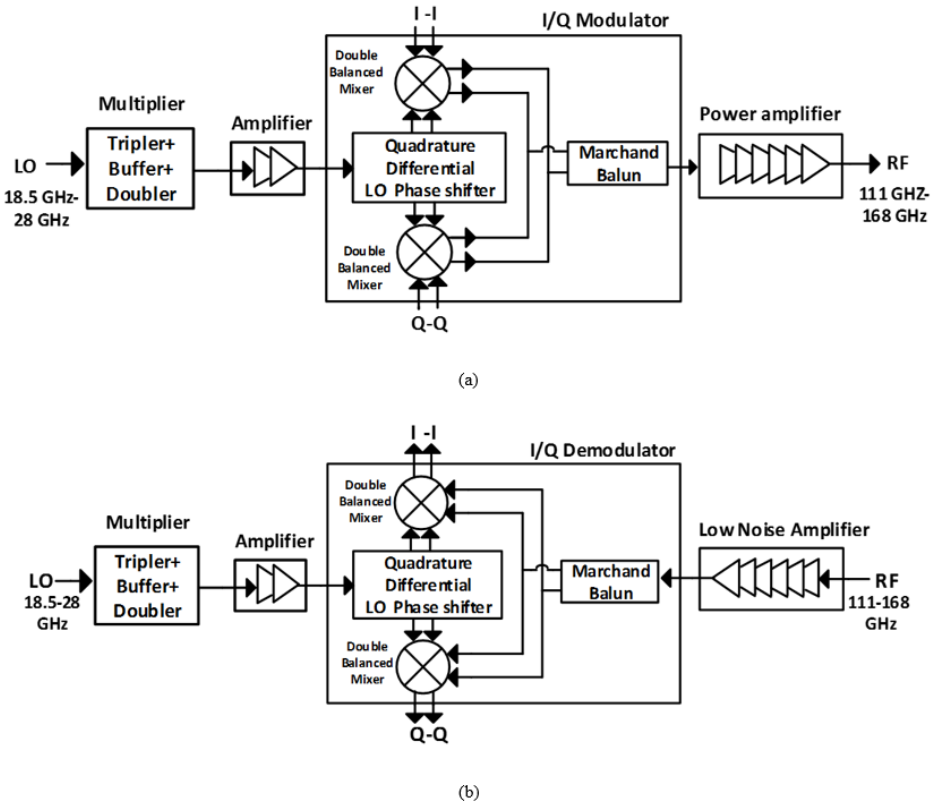


Fig. 1. The block diagram of direct conversion (a) I/Q transmitter and (b) I/Q receiver.

limeter wave wireless communications system demonstrators have been developed such as amplitude shift keying (ASK) [26], [27], on–off keying (OOK) [28], or binary phase-shift keying (BPSK) [29], [30] using simple and reliable modulation format with low spectrum efficiency (<1 bit/s/Hz). The spectral efficient complex modulation techniques, such as multi-level phase shift keying (PSK) or multi-level quadrature amplitude modulation (QAM) are reported in [31]–[40].

The design of highly integrated circuits at this frequency range is challenging as accurate modeling of active and passive components is required, and complex architectures have to be considered. In this paper, a fully integrated 110–155 GHz direct quadrature transmitter and receiver chipsets are described and implemented in a 130 nm SiGe BiCMOS technology for high data rate communication purpose. Concerning the maximum cut-off frequencies of the technology (ft/fmax of 250 GHz/370 GHz), a conventional fundamental Gilbert-cell I/Q mixer [41]–[43] along with the six-stage LNA/PA is chosen for the receiver/transmitter, respectively. The fundamental mixing approach combined with a fully differential circuit architecture offers a better performance in terms of high conversion gain, low dc-offset and LO leakage compared to the sub-harmonic technique [21]. The LO generation network consists of an X6 multiplier [44] followed by a two-stage driver amplifier. This configuration allows for designing the oscillator at one sixth of the fundamental D-band frequency. Consequently, the packaging of the transmitter/receiver chips are significantly simplified, resulting in a low-cost implementation. Furthermore, the quadrature arrangement of the chipsets attains a spectral efficient RF link supporting high-order modulation schemes, which makes it very attractive for multi-purpose applications. For example, presented chipset is designed for two application demonstrators, a telecom D-band radio link for the frequency band 141.5-148 GHz, and a radar sensor for the 122–123 GHz ISM-band. In order to cover both applications and frequency bands in one chip set, all sub-circuits are designed to have high bandwidth. The paper is organized as follows. Section II describes the design of transceiver chipset with the description of each building blocks. Details of the measurement set-up and results of the transmitter and receiver chips are described in Section III. Finally, Section IV summarizes the results and compares them with other published works.

II. FULL INTEGRATION OF TRANSMITTER AND RECEIVER CHIPSET IN D-BAND

The presented I/Q transmitter and receiver chipset is designed and fabricated in a 130 nm SiGe BiCMOS process from Infineon (B11HFC). The process features high-speed npn HBTs with maximum f_t/f_{max} of 250 GHz/370 GHz and BVCEO of 1.5 V [45]. The layer stack includes six levels of copper metalization and 1.0 μm aluminum as top metal which is suitable for analog mixed-signal millimeter wave designs. The silicon substrate thickness is 185 μm. In the presented designs, Metal2 is used as a ground layer and Metal3 to Metal6 are used for interconnections and designs of passive components. At millimeter waves, proper implementation of passive structures and their modeling accuracy become increasingly important for

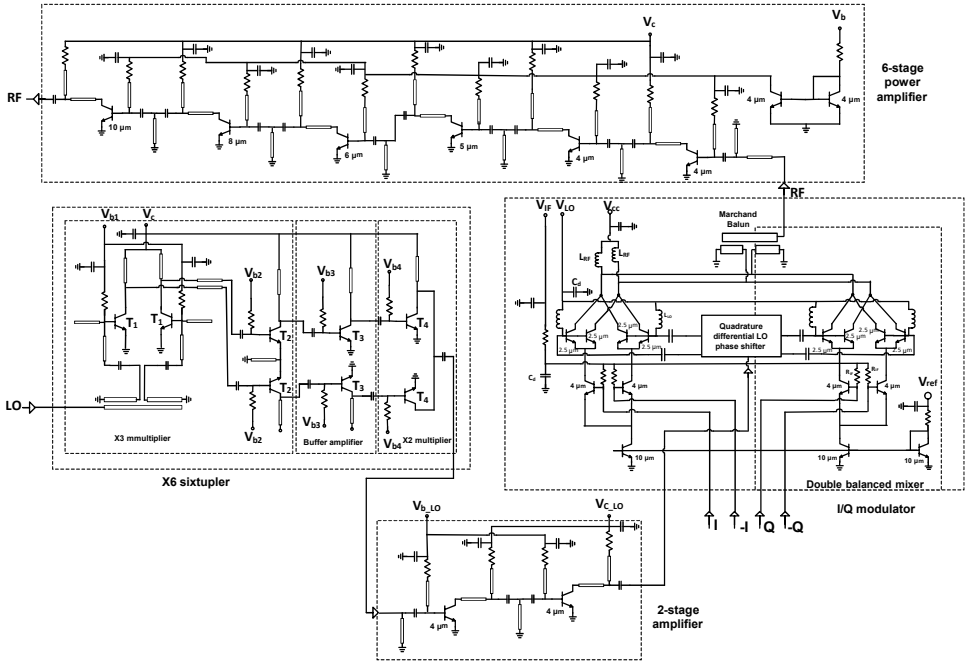


Fig. 2. Simplified schematic of direct conversion I/Q Transmitter.

the design success. Unlike conventional transmission line-based matching techniques commonly used for millimeter wave designs, we have implemented custom spiral inductors and used them together with a metal–insulator–metal (MIM) capacitor of the process to perform impedance matching and inductive loads. By taking advantage of multilayer metallization, this approach significantly reduces the consumed chip area. All other interconnects, even short lengths, are modeled as transmission lines and their effect is included in simulations. The presented circuits are designed using Cadence and the electromagnetic performance of critical layout parts are simulated with Sonnet. This section presents a brief description of the integration of front-end circuits into I/Q transmitter and receiver chipset. In both transmitter and receiver, each individual circuit is initially designed for standalone operation and then integrated in the complete transmitter and receiver chipset.

A. I/Q Transmitter

The transmitter is a direct modulation transmitter, comprising two double balanced (I and Q) mixers pumped by a frequency sixtupler for output frequencies from 110 GHz to 170 GHz. A two-stage D-band amplifier is used at the output of the frequency sixtupler to increase the input LO power to the I/Q mixer. The signals from the two I/Q mixers are added and amplified by a 6-stage power amplifier, see Fig. 1.

The simplified schematic diagram of the transmitter is shown in Fig. 2. The I/Q modulator is based on a recently published design [41], [46] and consists of two Gilbert mixer cells, an on-chip integrated differential LO coupler and RF and LO baluns. This configuration offers a high isolation between all three ports in a very compact die footprint. The topology of a quadrature balanced mixer requires generation and distribution of differential 90-degree phase-shifted millimeter-wave signals. Quadrature differential LO signals are generated with an on-chip differential coupler. This design is a differential implementation of the backward coupler [47]. In our designs, this is realized by including transmission-line-based baluns and a differential coupler on chip. Performance of all these passive components are electromagnetic (EM) simulated using Sonnet and imported into the circuit design environment for co-simulation. The input baseband signals are converted to current signals by the transconductance stages and are fed to the switching quads. For best switching performance, the mixer transistors are chosen to be 2.5 μm long and the lower transistors are accordingly scaled to be 4 um long. The operating condition is set by the reference current which is mirrored to the two mixer cells. Baseband ports are DC coupled as blocking capacitors for such frequencies may occupy very large chip area. Collector and base voltages of switches are applied to virtual RF grounds of the load and LO matching network respectively. Decoupling capacitors are added to avoid potential odd-mode instability of the circuit. In order to avoid the problems with the ground plane as mentioned above, fully differential signaling is used throughout the design. The lowest metal layer (Metal2) is however still included as the ground plane for better definition of common-mode signals in the electromagnetic simulations and to provide return path to the DC currents. In single sideband operation, the modulator demonstrates a maximum conversion gain of 9.8 dB with 3 dB RF bandwidth of 33 GHz (from 119 GHz to 152 GHz). The measured image rejection ratio (IRR) and LO suppression are 19 dB and 31 dB, respectively. The output P1dB is -4 dBm at 140 GHz RF and 1 GHz intermediate frequency (IF) and the chip consumes 53 mW dc power. The frequency sixtupler comprises of a frequency tripler, a buffer amplifier and a frequency doubler. The input signal is applied to a differential stage through a Marchand balun. To ensure sufficient LO

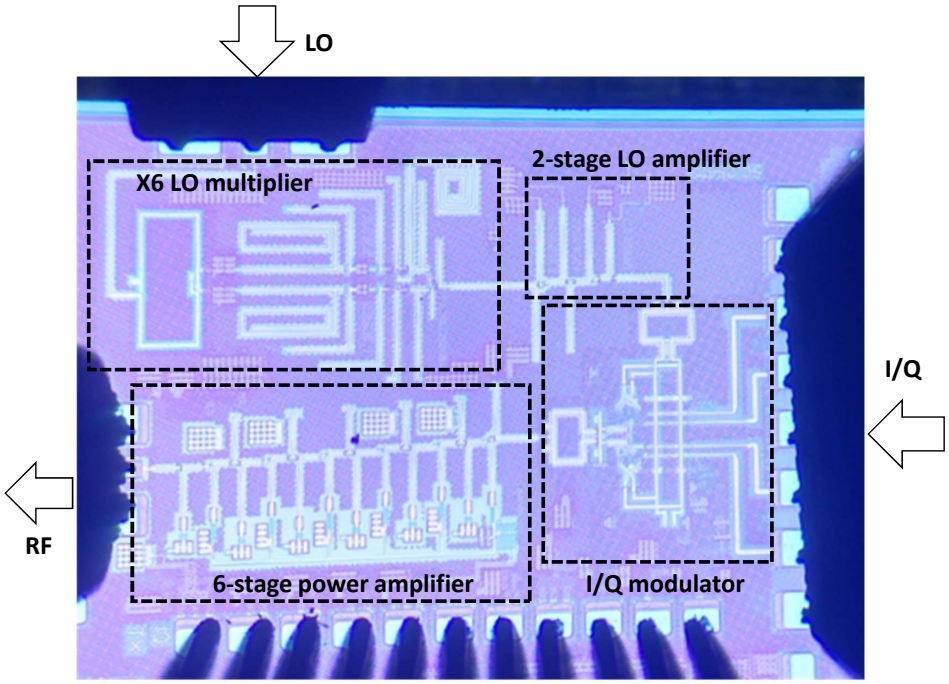


Fig. 3. The fabricated chip photo of direct conversion I/Q transmitter. The chip area is 1.4 x 1.1 mm^2.

power to the mixers, a two-stage LO amplifier is used at the output of frequency sixtupler to increase its output power. The tripler uses the concept of mixing the first and second harmonic to generate the third harmonic which increases output power and power efficiency. The output of the tripler is fed to the frequency doubler through a buffer amplifier. Transistors T1 and T2 have two emitter fingers with a length of 6.3 um. The other transistors have a single emitter finger with a length of 10 um. The sixtupler was measured separately on a breakout circuit, it has a bandwidth of 37 GHz (from 110 to 147 GHz) and a maximum output power of 4.5 dBm. More design detail of the sixtupler is published in [44]. A six-stage amplifier is used at the output of modulator to increase output power of the transmitter chip. The purpose is to provide a wideband operation and flat gain, rather than high output power, since the output signal is planned to be amplified with an external PA in a wireless link demonstrator [48]. The external PA is based on 8-way power combining and has demonstrated 13.5 dBm output power at 2 dB compression and a PAE of 5.5 percent at 140 GHz. A maximum power of 19 dBm was measured at 120 GHz with a PAE of 13.2 percent. The power consumption is 550 mW and the chip size 0.53 mm^2.

The six-stage amplifier in the transmitter design is based on a lossy-matching concept in order to ensure wideband operation. All six transistors are used in common-emitter configuration and share common base and collector voltage supplies.

The emitter lengths of the transistors are 4, 4, 5, 6, 8 and 10 μm respectively. A T-network with a shorted stub is used for inter-stage matching. The amplifier, measured as a stand-alone cutout for test, shows a 3 dB bandwidth of 115–155 GHz with a maximum gain of 19 dB. A current of 38 mA with $V_{cc} = 1.5$ V is used for bias, resulting in a power consumption of less than 60 mW. Its saturated output power is 7 dBm at 130 GHz. The current in six bases of transistors is set by using a current mirror.

The chip photograph is shown in Fig. 3. As annotated in the figure, the mixer cells including the transconductance stages and the switching quads are densely laid out in the center in order to minimize any unwanted parasitic effects. The LO distribution and phasing as well as the matching networks are all symmetrically planned around the mixing cells to maintain the amplitude and phase balance of the modulator as much as possible. The modulator, LO multiplier, LO amplifier and power amplifier are integrated in a compact footprint. The chip area including pads is 1.4 mm $\times$ 1.1 mm.

B. I/Q Receiver

The receiver is a direct conversion I/Q receiver consists of a six-stage low-noise amplifier, a double balanced I/Q mixer and a LO frequency multiplier chain. The LO multiplier chain includes frequency sixtupler followed by a two-stage amplifier, as shown in Fig. 1(b). The LO frequency multiplier chain in receiver is based on same design as in the transmitter. Before the complete receiver chip was integrated, the demodulator and low noise amplifier were designed and verified separately. The demodulator circuit consists of two double-balanced Gilbert-cell mixers, on-chip integrated differential LO coupler, and RF and LO baluns. All transistors in the circuit have minimum emitter width. The demodulator is presented in [42]. The RF port is impedance matched to 50 for interfacing to a low-noise amplifier. Inductance of the routing transmission lines proved to be sufficient to omit any spiral inductor at the RF port. This is advantageous to reduce the input ohmic loss, and therefore, noise of the circuit. Resistive IF loads are used to avoid the need for large on-chip inductors and to minimize the risk of instability. IF ports are isolated from the next stage by emitter followers,

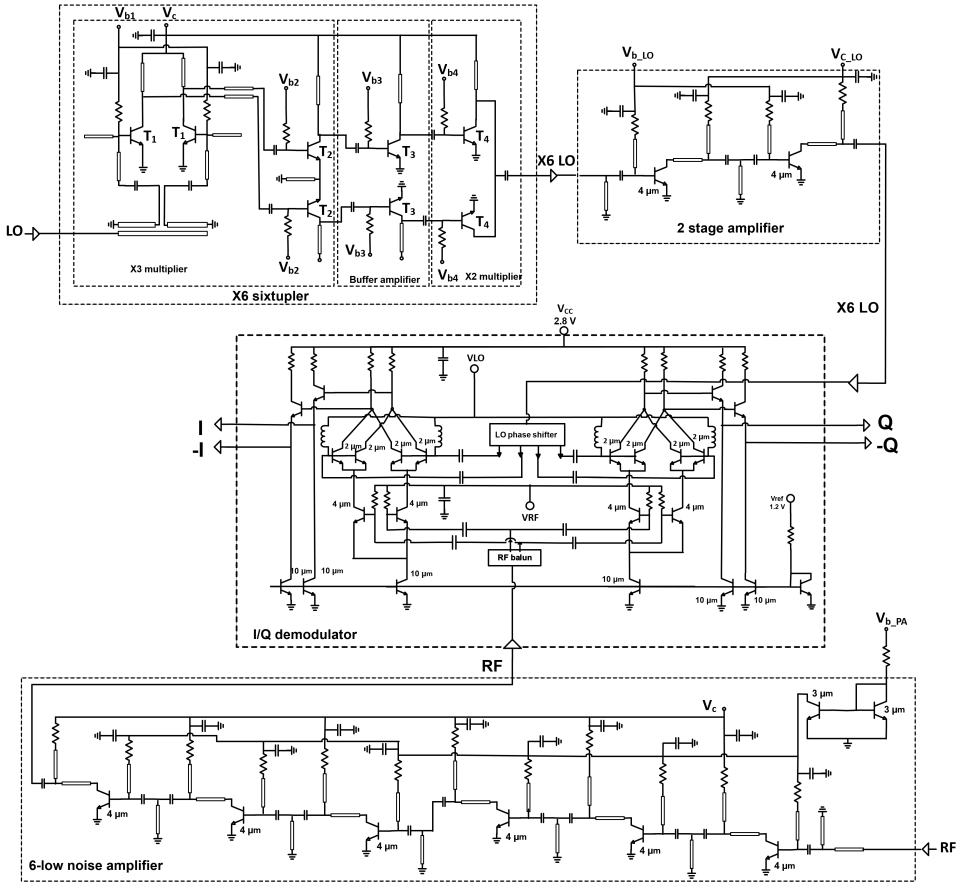


Fig. 4. Simplified schematic of direct conversion I/Q receiver.

which are also biased with current sources and are designed to match to 50 Ω over a broad bandwidth. The demodulator, characterized as an image reject mixer, exhibits 10 dB conversion gain with 23 dB image rejection ratio. The measured 3 dB RF bandwidth is 36 GHz and the IF bandwidth is 18 GHz. The active area is 620 μm $\times$ 480 μm including the RF and LO baluns.

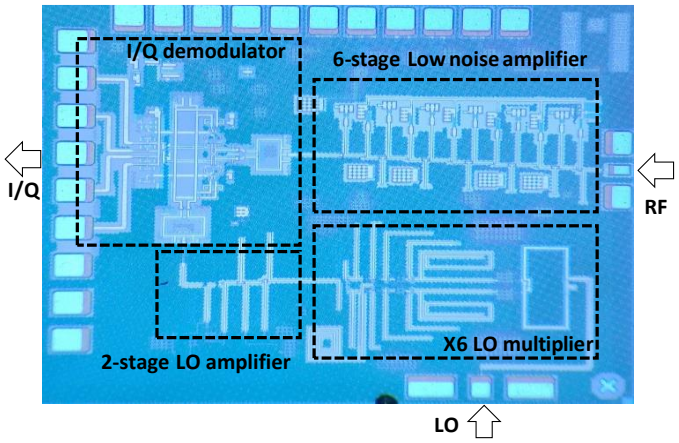
The low noise amplifier is a six-stage amplifier with 'lossy match' type matching utilizing resistively loaded stubs at the input and output of each amplifiers stage. Due to this topology it is possible to achieve a very wide bandwidth with full coverage of the D-band. A high 1 dB bandwidth of 117–162 GHz was achieved with a nominal gain of 18.9 dB. The measured gain is within 2 dB of the simulated gain from 120 to 180 GHz. The simulated noise figure is 10 dB. The outputs from the receiver chip are dc coupled differential I and Q signals and inputs are single ended LO and RF signals which are converted to differential before the demodulator. The single-ended LO and RF signals are converted to differential by on-chip Marchand baluns. The simplified schematic is shown in Fig. 4. Fig. 5(a) shows a photograph of the fabricated receiver MMIC. The chip size is 1.4×1.1 mm^2. Bias voltages are shown in figure where the dc bias feed lines are properly RF decoupled to avoid unwanted feedback and combined to reduce the number of dc pads. The optimum operation condition is set by providing proper base currents to the amplifier and frequency multiplier, while the current of modulator is set by VRef of the current mirror which is mirrored to two mixer cells, as shown in Fig. 4. The base bias to RF differential pair and LO quad is applied through resistors and inductors, respectively. The collector voltage of 2.7 V is applied to two mixing cells and emitter followers, where mixer cells draw 8.5 mA and emitter followers draw 16 mA of current.

III. MEASUREMENT OF THE TRANSMITTER AND RECEIVER

This section presents the characterization of I/Q transmitter and receiver chips as a single sideband transmitter and image reject receiver, respectively. The measurements of the individual building blocks were conducted in optimized bias conditions. To reduce the complexity for the biasing effort of the receiver MMIC, the degree of different bias conditions has been reduced, as a result, the overall power consumption of the receiver differs from the sum of the individual building block power consumptions.

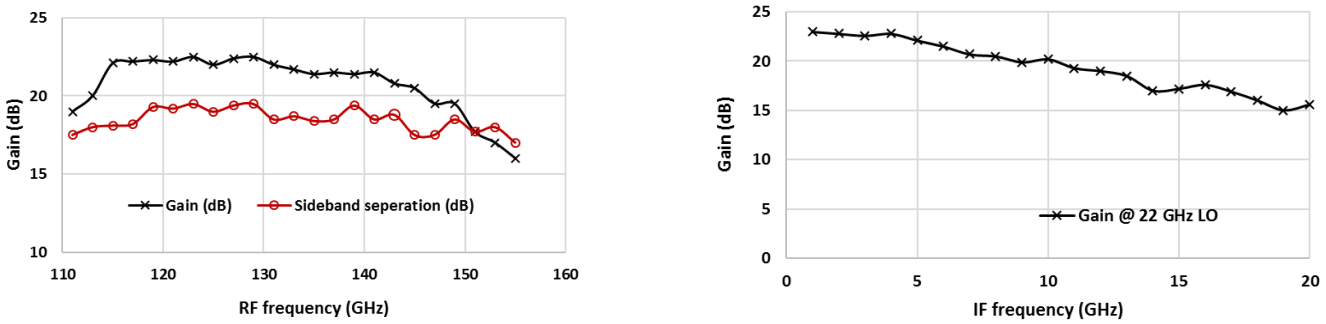
A. Test Set-up

The chips are measured on a probe station with wafer probes. On the RF port, a GSG probe with 75 µm pitch and WR6.5 waveguide interface and on the LO port, a 100 µm GSG probe with coaxial connector are used. For the differential baseband input/output signals a quad GSSGSSG probe with 125 µm pitch is used. To characterize the mixer performance, on-wafer measurements are carried out. The RF signal is generated and calibrated using a Keysight PNA-X N5247A microwave



(a) (b)

Fig. 5. (a) The fabricated chip photo of direct conversion I/Q receiver. The chip area is 1.4 x 1.1 mm2. (b) Simplified block diagram of measurement setup for characterization of the transmitter MMIC chip.



(a) (b)

Fig. 6. (a) Transmitter measured upper sideband gain and sideband suppression versus RF frequency. (b) Transmitter measured gain versus IF frequency at fixed 22 GHz LO.

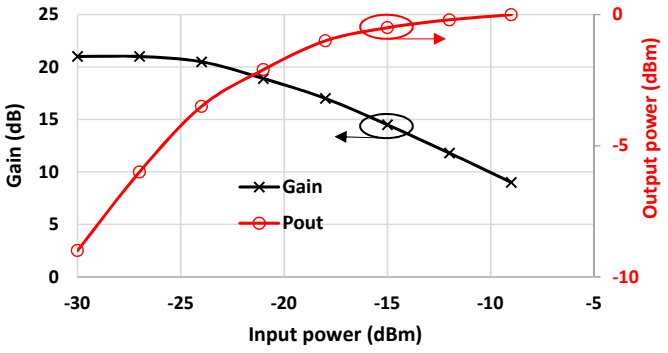


Fig. 7. Transmitter measured output power and gain at 139 GHz versus input power at 1 GHz.

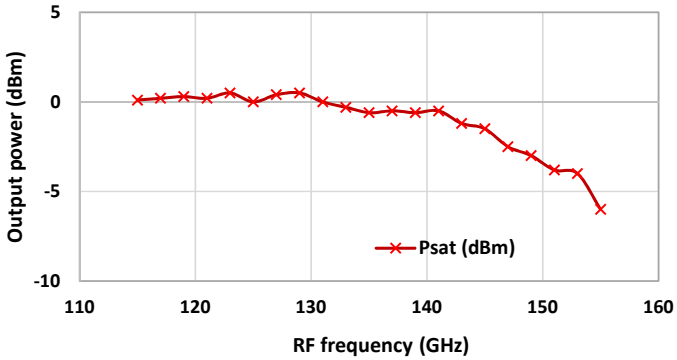


Fig. 8. Measured saturated output power of the transmitter versus RF output frequency at an input frequency of 1 GHz.

network analyzer from 10 MHz to 26.5 GHz and a WR6.5 (110–170 GHz) frequency converter module extender from Virginia Diodes, Inc. to extend the frequency range from 110 to 170 GHz. The LO signal is provided from an Agilent E8257D, 250 kHz to 67 GHz PSG signal generator. The measurement set up is shown in Fig. 1(b). In the direct conversion transmitter and receiver mode, the four baseband signals are applied as differential I and Q baseband signals. In single side band and image

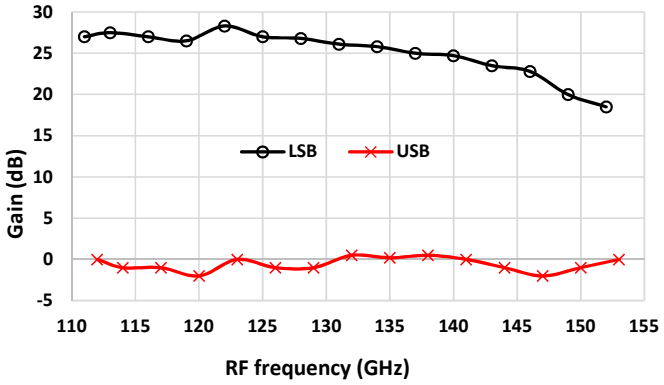


Fig. 9. Receiver measured conversion gain of upper sideband (USB) and lower sidebands (LSB) over RF frequency at 1 GHz IF.

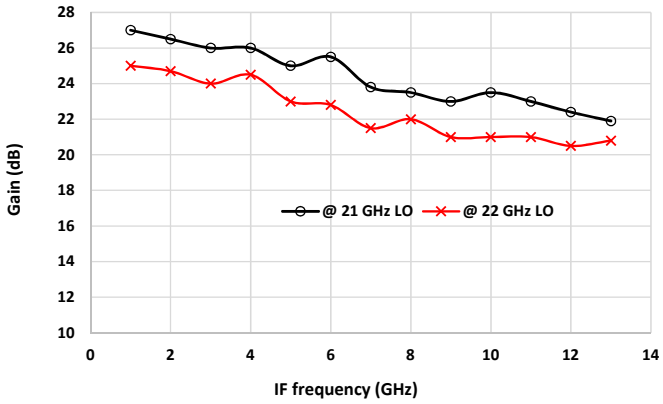


Fig. 10. Receiver measured gain versus IF frequency at fixed LO.

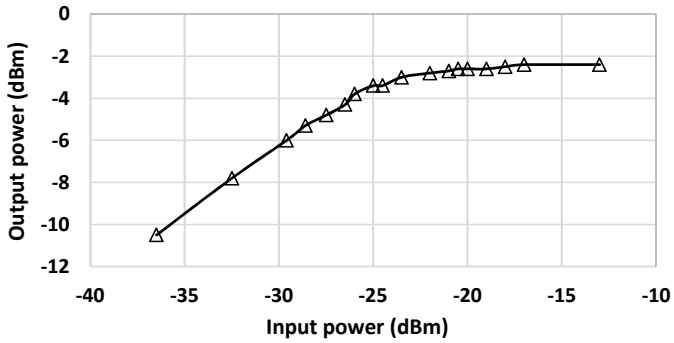


Fig. 11. Receiver measured output power at 1 GHz versus input power at 132 GHz.

reject frequency converter mode however, they represent four phases of the IF signal. Assuming that amplitude and phase balance of these hybrids are ideal, the measured sideband suppression and image rejection ratio are indicative of amplitude and phase balance of the transmitter and receiver chips. These external components and connecting cables are however not ideal and contribute to the measured imbalance.

Imperfections of the external hybrids are specified by the manufacturer to be ± 0.6 dB and ± 10 degree, respectively from 1 to 18 GHz. This error is embedded in the presented results of the chipset.

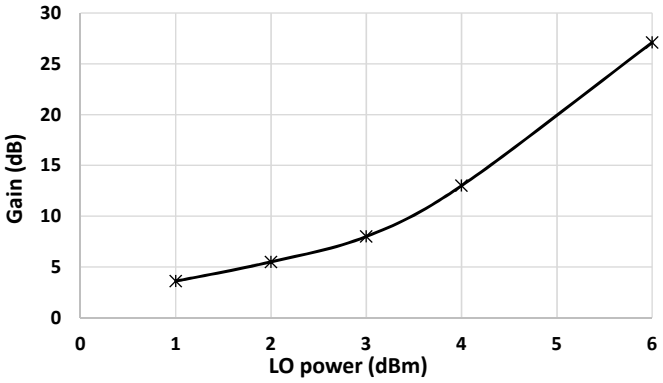


Fig. 12. Receiver measured gain versus LO input power at 130 GHz and 1 GHz IF.

B. Transmitter Results

The transmitter is characterized in single side band mode, and parameters like the upper sideband conversion gain, side band suppression, P1 dB gain compression point, and saturated output power are presented in this section. An input IF signal of 1 GHz with -30 dBm is applied to IF port. The LO input signal with 6 dBm power is varied from 18.5 to 28 GHz. The measured conversion gain for the upper sideband versus RF frequency is shown in Fig. 6(a). A conversion gain of 22±1 dB is achieved from 114 GHz to 145 GHz. The unwanted sideband is suppressed by 18–25 dBc.

The IF bandwidth is measured by varying input signal frequency from 1 to 18 GHz at a fixed LO of 22 GHz. The measured conversion gain variation is shown Fig. 6(b). The transmitter is providing relatively flat gain up to 16 GHz where the gain drops by 5 dB. This is believed to be dominantly due to the upper frequency limitation of the external hybrids and not the chip itself.

Fig. 7 shows the output power and conversion gain at 139 GHz versus input power at 1 GHz. The output P1dB is measured -4 dBm. It can be seen from Fig. 8, that the maximum output power is 0±0.5 dBm from 115 GHz to 140 GHz. The total dc power consumption of transmitter chip is 240 mW.

C. Receiver Results

The conversion gain of the receiver chip is measured at an input RF signal power of -30 dBm and the frequency is varied from 111–168 GHz. The input LO power is 6 dBm. At each RF frequency, the LO frequency is switched above and below the RF in order to measure conversion gain in both lower and upper sidebands. The measured results are shown in Fig. 9. As can be seen, the measured maximum gain is 27 dB. The 5 dB RF bandwidth is 26 GHz from 112-146 GHz. The ratio of the two output powers is defined as the image rejection ratio (IRR) and is 24 dB for most of the RF frequencies. Depending on application, upper and lower sidebands can be switched by switching external 900 hybrid network in Fig. 5(b). The measured gain versus IF frequency is shown in Fig. 10 at a fixed LO frequencies of 21 GHz and 22 GHz. The measured 5 dB IF bandwidth of the receiver is 13 GHz which is again believed to be limited by the external hybrid network.

Fig. 11 shows the measured output power at 1 GHz versus input power at RF 132 GHz. The receiver can provide up to -3 dBm of saturated output power. The gain versus input LO power at 130 GHz and IF at 1 GHz is shown in Fig. 12. The total dc power dissipation is 192 mW.

IV. CONCLUSION AND PERFORMANCE COMPARISON

A fully integrated multifunctional direct conversion I/Q transmitter and receiver chipset for application in a millimeter-wave communication and imaging system operating in 110–170 GHz has been designed and verified experimentally. The chipset is fabricated using a commercial 130 nm SiGe BiCMOS process and can be used in both homodyne and heterodyne architectures. The chipset exhibits good overall conversion gain, operates over wide bandwidth, and has an acceptable noise figure. Table I and II show the comparison of millimeter-wave transmitter and receiver, respectively. The presented chipset has largest RF bandwidth and IF bandwidth and consume low dc and LO power among published millimeter-wave transmitter/receiver operating in D-band and F-band (90–140 GHz). The chip area of each transmitter and receiver circuit is $1.4 \times 1.1\ \mathrm{mm}^2$. It can nevertheless be seen that the presented designs demonstrate outstanding performance in terms of conversion gain, and RF/IF bandwidth for the given technology. Due to the high bandwidth, the amplifier can be used for both the telecom demonstrator and the sensor demonstrator at 122–123 GHz ISM-band.

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Table 1. Perormance comparison of down-converter circuits

Frequency (GHz)	Integration	Conversion gain (dB)	Noise figure (dB)	Input P1dB (dBm)	LO power (dBm)	dc power (mW)	Technology (f_t/f_{max}) (GHz/GHz)	Ref
122	LNA+Mixer+VCO+divider	31	11	-44	9	370	130 nm SiGe (255/315)	[14]
115-122	LNA+I/Q demodulator+IF Amp.	10.5-13.5	10-11.5	-20	-	130	130 nm SiGe (230/280)	[7]
120-145	LNA+I/Q demodulator	3	5–6 (Sim)	-0.5	-	120	100 nm GaAs (200/300)	[49]
144	LNA+Mixer+X3	48	12.5	-	-	214	65 nm CMOS	[50]
158-165	LNA+I/Q demodulator	20-25	11-14	-	-	1400	SiGe (260/380)	[51]
150-162	LNA+I/Q demodulator+divider	34	8.5	-35	-	490	250 nm SiGe (230/350)	[15]
150-165	LNA +Mixer	27.5	9.5	-	-8	160	SiGe (260/350)	[52]
112-140	**LNA + I/Q demodulator +X6**	**27**	**10 (simulated)**	$\mathbf{-24}$	**6**	**280**	**130 nm SiGe (230/280)**	**this work**

Table 2. Performance comparison of up-converter circuits

Frequecy (GHz)	Integration	Conversion Gain (dB)	RF Bandwidth (dB)	Output Power (dBm)	dc Power (mW)	Technology (f_t/f_{max}) (GHz/GHz)	Ref
75–95	I/Q modulator+6 stage PA	8.5	20	6.6	120	65nm CMOS	[53]
144	mixer+5 stage PA	9.7	-	10.1	219	65nm CMOS	[50]
150–168	I/Q modulator+3stage PA+divider	34	18	10.6	610	250 nm SiGe (230/350)	[15]
114–145	**I/Q modulator+6 stage PA+X6**	**23**	**30**	**0**	**240**	**130 nm SiGe (230/280)**	**this work**

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Sona Carpenter received the M.E. (Hons.) degree in Electronics and Telecommunication from the S. G. S. Institute of Technology and Science, Indore, India, in 2008, and Ph.D. degree from the Chalmers University of Technology, Goteborg, Sweden, in 2018. In 2007, she joined the Satellite Payload Technology Area, Indian Space Research Organization, Ahmedabad, India, where she was a Scientist/Engineer involved with research and development of microwave circuits and subsystems for the Indian national and geostationary communication satellite payload receivers. She was a Postdoc Researcher with the Microwave Electronic Laboratory, Chalmers University of Technology in 2019. Her Ph.D. and Postdoc Research include the design of millimeter-wave integrated circuits and systems with a focus on millimeter-wave high-speed wireless communication. Ms. Carpenter was a recipient of the 2013 GaAs Association Ph.D. Student Fellowship Award. Since 2019, she has been with Sivers Semiconductors, AB, Göteborg, Sweden.

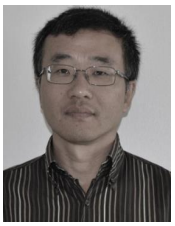


Herbert Zirath was born in Göteborg, Sweden, on March 20, 1955. He received the M. Sc and Ph. D. degree in Electrical Engineering from Chalmers University, Göteborg, Sweden, in 1980 and 1986, respectively. From 1986 to 1996 he was a Researcher at the Radio and Space Science at Chalmers University, engaged in developing a GaAs and InP based HEMT technology, including devices, models and circuits. In the spring-summer 1998 he was Research Fellow at Caltech, Pasadena, USA, engaged in the design of MMIC frequency multipliers and Class E Power amplifiers. He is since 1996 Professor in High Speed Electronics at the Department

of Microtechnology and Nanoscience, MC2, at Chalmers University. He became the head of the Microwave Electronics Laboratory 2001. At present he is leading a group of approximately 40 researchers in the area of high frequency semiconductor devices and circuits. His main research interests include MMIC designs for wireless communication and sensor applications based on III-V, III-N, Graphene, and silicon devices. He is author/co-author of more than 570 refereed journal/conference papers, h-index of 37, and holds 5 patents. He is research fellow at Ericsson AB, leading the development of a D-band (110-170 GHz) chipset for high data rate wireless communication. He is a co-founder of Gotmic AB, a company developing highly integrated frontend MMIC chip-sets for 60 GHz and E-band wireless communication.



Zhongxia Simon He received the M. Sc. degree from Beijing Institute of Technology, Beijing, China, and the Ph. D. degree from Chalmers University of Technology, Göteborg, Sweden, in 2008 and 2014, respectively. He is currently an Assistant Professor with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience (MC2), Chalmers University. His current research interests include high data rate wireless communication, modulation and demodulation, mixed-signal integrated circuit design, radar, and packaging. .



Mingquan Bao received the B.S. and M.S. degrees in Electrical Engineering from Zhejiang University, Hangzhou, China, in 1985 and 1988, respectively, and the Ph.D. degree in radar remote sensing from the University of Hamburg, Hamburg, Germany, in 1995. From 1995 to 1997, he was with the Institute of Oceanography, University of Hamburg. From 1997 to 2000, he was with the Center for Remote Imaging Sensing and Processing, University of Singapore, Singapore. From 2000 to 2001, he was with the German Aerospace Center (DLR), Köln, Germany, where his research was focused on interferometric radar remote sensing. Since 2001, he has been with Radio Access Hardware, Device and EMF, Ericsson Research, Ericsson AB, Göteborg, Sweden. He has authored over 50 papers in refereed journals and conferences. He holds 41 U.S., European, Japan, and China patents. He is a recipient of the Tatsou Itoh best paper award from IEEE Microwave and Wireless Components Letters, 2016. His research interests include RF integrated circuit (RFIC) designs such as low-noise amplifiers (LNAs), mixers, frequency multipliers, power detectors, power amplifiers, and voltage-controlled oscillators (VCOs) in silicon, GaAs, InP, GaN technologies.